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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/886,625	07/01/97	SHENOY N	SNSY-A1996-0

EXAMINER	
GARBOWSKI, L	
ART UNIT	PAPER NUMBER
2768	10

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DATE MAILED: 08/16/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
08/886,625	SHENOY et al.
Examiner	**Group Art Unit**
Garbowski	2768

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication .
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☒ Responsive to communication(s) filed ~~on~~ thru 2.7.00.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1-14, 18-21 is/are pending in the application.

Of the above claim(s)_____ is/are withdrawn from consideration.

☐ Claim(s)_____ is/are allowed.

☒ Claim(s) 1-14, 18-21 is/are rejected.

☐ Claim(s)_____ is/are objected to.

☐ Claim(s)_____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on_____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on_____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number)_____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received:_____.

Attachment(s)

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 6

☐ Interview Summary, PTO-413

☒ Notice of Reference(s) Cited, PTO-892

☐ Notice of Informal Patent Application, PTO-152

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Other_____

Office Action Summary

1. This office action is in response to the communication filed 02/07/00.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 5-10, 12-14 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hathaway et al. [U.S. Patent #5,757,657] in view of Shouen [U.S. Patent #6,086,625].

4. As per claim 1, Hathaway et al. teach a computer controlled method for placing cells [see the entire document, at least as cited] comprising a) generating a netlist through a synthesis process [column 2, lines 35-37]; b) executing a cell separation process according to the netlist [column 2, lines 52-53]; c) changing the netlist [column 2, lines 17-19]; d) modifying spacings of the cells responsive to changes made to the netlist [column 3, lines 17-28, 45-64]; e) partitioning the cells into a plurality of partitions [column 2, lines 39-45]; f) changing placements of the cells after a partition is created [column 4, lines 13-27]; and g) determining whether the placement has converged [column 2, lines 45-49], wherein steps c-f are repeated if convergence is not yet achieved [column 1, lines 65-67]. However, Hathaway et al. do not teach wherein steps b-g are performed as part of a rough placement process. Shouen teaches a computer controlled method for placing cells, comprising wherein a rough placement process [please see the entire document, at least at

column 7, line 44-column 10, line 43]. Therefore, a person of ordinary skill in the art at the time of the invention would have found it obvious to employ the computer controlled method for placing cells comprising the steps taught by Hathaway et al. as part of a rough placement process because "it is possible to realize an increase of an yielding rate and a reduction of a cost in the fabrication of the circuit. As this, the method and apparatus of this invention are extremely advantageous when an electronic circuit whose scale will be increased more and more in the future is designed and fabricated" [column 15, lines 7-12]. As per claim 2, Hathaway et al. further teach changing size in response to changes made to the netlist [column 3, lines 17-28; column 5, lines 51-65; column 7, lines 27-35]. As per claim 3, Hathaway et al. further teach inputting HDL, user constraints, and technology data into the synthesis process [column 1, lines 13-17; see also applicant's specification at page 2, line 24 through page 3, line 1, page 7, lines 15-22]. As per claim 5, Hathaway et al. further teach wherein the cell separation process assigns an (x,y) location to each of the cells of the netlist [column 2, lines 52-53]. As per claim 6, Hathaway et al. further teach wherein the netlist is changed based on cell location information [column 2, lines 17-19, 50-54; column 3, lines 44-50]. As per claim 7, Hathaway et al. further teach wherein a change to the netlist includes sizing a gate up or down [column 2, lines 17-19]. As per claim 8, Hathaway et al. further teach wherein a change to the netlist includes adding or deleting one or more gates [column 2, lines 17-19]. As per claim 9, Hathaway et al.

further teach wherein convergence is achieved when each partition has a number of cells less than a pre-determined value [column 7, lines 30-35].

5. As per claim 10, Hathaway et al. teach a computer system including a processor coupled to a bus and a memory coupled to the bus [see the entire document, at least as cited] comprising: means for assigning locations to each of the cells of the netlist [column 2, lines 52-53]; means for changing the netlist in response to cell location information [column 2, lines 17-19], wherein an area is allowed to be scaled in response to changes made to the netlist [column 5, lines 51-65]; means for partitioning the cells into a plurality of separate partitions, wherein cells are placed at different locations when a new partition is created [column 2, lines 39-45; column 4, lines 13-27]; means for changing the partitions, wherein the changes to the partitions result in corresponding changes to locations of where the cells are placed [column 3, lines 17-28, 45-64]; and means for determining convergence is achieved [column 2, lines 45-49]. However, although Hathaway et al. teach logic for placing cells of an integrated circuit design represented as a netlist having cells and connections between cells, Hathaway et al. do not specifically use the term rough placement logic. Shouen teaches a computer system comprising a rough placement logic [please see the entire document, at least at column 7, line 44-column 10, line 43]. Therefore, a person of ordinary skill in the art at the time of the invention would have found it obvious to employ the logic of Hathaway et al. as a rough placement logic because "it is possible to realize an increase of an yielding rate and a reduction of a cost in

the fabrication of the circuit. As this, the method and apparatus of this invention are extremely advantageous when an electronic circuit whose scale will be increased more and more in the future is designed and fabricated" [column 15, lines 7-12]. As per claim 12, Hathaway et al. further teach wherein a change to the netlist includes sizing a gate up or down [column 2, lines 17-19]. As per claim 13, Hathaway et al. further teach wherein a change to the netlist includes adding or deleting one or more gates [column 2, lines 17-19]. As per claim 14, Hathaway et al. further teach wherein convergence is achieved when each partition has a number of cells less than a pre-determined value [column 7, lines 30-35].

6. As per claims 18-20, the combination of Hathaway et al. [column 1, lines 15-16] and Shouen [figure 2] teach a computer-readable medium having stored thereon instructions for causing a computer to implement a placement process as outlined in the rejection of claims 1-3 above. The claims are considered rejected based upon the reasoning outlined above, and such is omitted here for sake of brevity.

7. Claims 4, 11 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hathaway et al. in view of Shouen, and further in view of applicant's specification.

8. The above combinations teach the features from which the claims depend, but do not teach a mapped netlist. The specification teaches that "any of the synthesis tools commercially available ... can be used to generate the mapped netlist" [page 7, lines 16-18]. Therefore, considering the high level of ordinary skill in the art, a person of ordinary

skill in the art at the time of the invention would have found it obvious to modify the Hathaway et al. teaching to include a mapped netlist because the ready availability of this feature facilitates and uniforms the design placement process.

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

10. Wang et al. [U.S. Patent #5,818,729] disclose placing cells including rough placement and partitioning.

11. Gelatt, Jr. et al. [U.S. Patent #4,495, 559] disclose optimizing the placement of cells including partitioning.

REMARKS

12. Applicant's arguments against the Hathaway et al. reference have been fully considered but are not deemed persuasive. With respect to claim 10, the applicant argues "The rough placement logic comprises ..." [page 5, paragraph 4, lines 3-5], yet the language of the claim clearly does not recite such an interpretation of the subject matter. With respect to claim 1, the applicant does not offer an argument. At page 6, paragraph 2, the applicant argues "rough placement process", specifically that the significance of the invention is that changes occur during a rough placement process, however, the examiner does not see the significance in the claim language. Merely including "rough placement" in the claims does not adequately describe the subject matter, the scope of the specific features recited does not appear to describe any significance other than that which is shown as rejected above.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leigh Marie Garbowski whose telephone number is (703) 305-9753.

14. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Leigh Marie Garbowski
August 9, 2000

Paul R. Lintz
Primary Examiner